**Commands**

**Simulation command**

* vcs +v2k –gui design\_file.v tb.v
* ./simv –gui
* vcs +v2k –debug\_all –gui –y /apps/toshiba/sjsu/verilog/tc240c +libext+.tsbvlibp tb.v design\_netlist.v
* dc\_shell –f synthesis.script | tee log.txt
* design\_vision & DVE

**RCA Synthesis Script**

Set link\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25 /apps/synopsys/SYNTH/libraries/syn/dw02.sldb /apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

Set\_target\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25}

read\_verilog RCA64.v

current\_design RCA64

check\_design

create\_clock clock -name clock -period 18.5600000

set\_propagated\_clock clock

set\_clock\_uncertainty 0.25 clock

set\_propagated\_clock clock

set\_fix\_hold [ get\_clocks clock ]

compile -map\_effort medium -incremental\_mapping

update\_timing

set\_max\_area 2500

report -cell

report\_timing -max\_paths 10

report\_area

report\_power

write -hierarchy -format verilog -output RCA64\_1\_nl.v

quit

**CLA-2L Synthesis.script**

set link\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25 /apps/synopsys/SYNTH/libraries/syn/dw02.sldb /apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

set target\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25}

read\_verilog {CLA4.v,CLA4\_2.v,CLA16.v CLA16\_2.v,CLA\_64.v}

current\_design CLA\_64

check\_design

create\_clock clock -name clock -period 4.9500000

set\_propagated\_clock clock

set\_clock\_uncertainty 0.25 clock

set\_propagated\_clock clock

set\_fix\_hold [ get\_clocks clock ]

compile -map\_effort medium -incremental\_mapping

update\_timing

set\_max\_area 2500

report -cell

report\_timing -max\_paths 5

report\_area

report\_power

write -hierarchy -format verilog -output CLA\_64\_1\_nl.v

quit

**CSAEQG Synthesis script**

set link\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25 /apps/synopsys/SYNTH/libraries/syn/dw02.sldb /apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

set target\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25}

read\_verilog {mux\_carry.v,mux\_sum.v,CSA64EQG.v}

current\_design CSA64EQG

check\_design

create\_clock clock -name clock -period 5.200000

set\_propagated\_clock clock

set\_clock\_uncertainty 0.25 clock

set\_propagated\_clock clock

set\_fix\_hold [ get\_clocks clock ]

compile -map\_effort medium -incremental\_mapping

update\_timing

set\_max\_area 3100

report -cell

report\_timing -max\_paths 5

report\_area

report\_power

write -hierarchy -format verilog -output CSA64EQG\_1\_nl.v

quit

**CSAUEQG Synthesis.script**

set link\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25 /apps/synopsys/SYNTH/libraries/syn/dw02.sldb /apps/synopsys/SYNTH/libraries/syn/dw01.sldb}

set target\_library {/apps/toshiba/sjsu/synopsys/tc240c/tc240c.db\_WCCOM25}

read\_verilog {FA.v,CSA2.v,CSA3.v,CSA4.v,CSA5.v,CSA6.v,CSA7.v,CSA8.v,CSA9.v,CSA10.v,CSA11.v,CSA64UEQG.v}

current\_design CSA64UEQG

check\_design

create\_clock clock -name clock -period 8.00000

set\_propagated\_clock clock

set\_clock\_uncertainty 0.25 clock

set\_propagated\_clock clock

set\_fix\_hold [ get\_clocks clock ]

compile -map\_effort medium -incremental\_mapping

update\_timing

set\_max\_area 3200

report -cell

report\_timing -max\_paths 5

report\_area

report\_power

write -hierarchy -format verilog -output CSA64UEQG\_nl.v

quit